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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,875	06/04/2001	Christophe de Dinechin	10011596-1	5117

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EXAMINER	
VO, LILIAN	

ART UNIT	PAPER NUMBER
2195	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,875	DE DINECHIN ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 26 are pending.

2. In view of the appeal brief filed on 12/05/05, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:

(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,

(2) request reinstatement of the appeal.

If reinstatement of the appeal is requested, such request must be accompanied by a supplemental appeal brief, but no new amendments, affidavits (37 CFR 1.130, 1.131 or 1.132) or other evidence are permitted. See 37 CFR 1.193(b)(2).

Claim Objections

3. **Claim 26** is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. Claim 26 recites the context is stored in memory other than the inconsequential register, which depends on claim 1 claiming to save the context using an inconsequential register. The uses of the memory other than the inconsequential register as recited in claim 26 is contradicting with its

parent claim. See also MPEP. 608.01 (n), "Infringement Test" for dependent claims. The test for a proper dependent claim is whether the dependent claim includes every limitation of the parent claim. The test is not whether the claims differ in scope. A proper dependent claim shall not conceivably be infringed by anything which would not also infringe the basic claim.

Claim Rejections - 35 USC § 101

4. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 1 – 11, 22 – 26 are rejected under 35 U.S.C. 101 because they are directed to non-statutory subject matter.

6. **Claims 1 – 11 and 23 – 26** are directed to method steps, which can be practiced mentally in conjunction with pen and paper, therefore they are directed to non-statutory subject matter. Specifically, as claimed, it is uncertain what performs each of the claimed method steps. Moreover, each of the claimed steps, inter alia, saving, preventing, restoring, using, can be practiced mentally in conjunctions with pen and paper. The claimed steps do not define a machine or computer implemented process [see MPEP 2106]. Therefore, the claimed invention is directed to non-statutory subject matter. (The examiner suggests applicant to change "method" to "computer implemented method" in the preamble to overcome the outstanding 35 U.S.C. 101 rejection).

7. **Claim 22** claims software which comprising instructions for performing context switch function. These instructions are not tangibly embodied in a manner so as to be executable.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 2, 3 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Bitar et al. (US Pat. 5,872,963, hereinafter Bitar).

10. Regarding **claim 1,** Bitar discloses a method of switching context on a processor (abstract, col. 12 lines 50 - 53), the method comprising:

saving the context under software control using an inconsequential register (col. 13 lines 57 – 65, col. 17 lines 39 – 41, 63 – 65, col. 18 lines 1 - 16); and

preventing the processor from changing the context while the context is being saved (col. 13 lines 57 – 65, col. 17 lines 65 – 67, col. 18 lines 17 - 24).

11. Regarding **claim 2,** Bitar discloses the inconsequential register is used as a temporary storage in lieu of a privileged register (col. 13 lines 59 - 60).

12. Regarding **claim 3**, Bitar discloses the context is saved at a predetermined interruption point (col. 13 lines 53 – 60, col. 17 lines 34 – 58 and 62 – 67).

13. **Claim 9** is rejected on the same ground as stated in claim 1 above.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 4 – 5 and 24 - 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bitar et al. (US Pat. 5,872,963) as applied to claim 1 above, in view of Bugion et al. (US 6,496,847, hereinafter Bugion).

16. Regarding **claim 4,** Bitar discloses the context switching between the execution entities (abstract, col. 13 lines 50 - 52). Bugion discloses the context is switched between a host operating system and a virtual machine application (Bugion: col. 4, lines 52 – 61: switching from HOS context to VMM context. Col 11, lines 30 – 52), the virtual machine application controlling the context switch (col. 11, lines 30 – 52: VMM handles directly all exceptions and interrupts that occur while executing in the VMM context. Col. 12, lines 20 – 24: the VMM completely takes over the machine and only voluntarily relinquishes control to the HOS). Therefore, it would have been obvious for one of an ordinary skill in the art, to relate Bugion's

teaching together with Bitar to efficiently perform the context switching between the execution entities as required.

17. Regarding **claim 5,** Bitar discloses the use of inconsequential register (col. 13 lines 59 – 60). Bugion discloses any available memory space is used to pass information to the virtual machine application (Bugion: col. 11, lines 30 – 52: total switch saves HOS context to any available memory space and changes the address space to be mapped into the VMM context. Col. 16, lines 45 - 61). Therefore, it would have been obvious for one of an ordinary skill in the art, to incorporate Bugion's teaching together with Bitar to utilize the available memory to save the context when a context switch occurs and still able to perform the intended functions equally well without causing the system to crash (Bugion: col. 11 lines 30 – 52).

18. Regarding **claim 24,** as modified Bitar discloses the inconsequential register includes storing an address, the address indicating a memory location at which the context will be saved (Bitar: fig. 3 and 4, Bugion: col. 11, lines 41 – 46, col. 14, lines 4 – 6).

19. Regarding **claim 25,** as modified Bitar discloses the inconsequential register does not store context a predetermined interruption point (Bugion: col. 8, lines 36 – 39, col. 16, lines 36 – 42).

20. Regarding **claim 26,** as modified Bitar discloses the context is stored in memory other than the inconsequential register (Bugion: col. 11, lines 30 – 52: any available memory space may be used to save context and actual storage).

21. Claims 6 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bitar et al. (US Pat. 5,872,963), as applied to claim 1 above, and in view of Applicants' admitted prior art (hereinafter AAPA).

22. Regarding **claim 6,** Bitar did not clearly disclose the context switched is using an IA-64 processor. However, an IA-64 processor is considered a well-known architecture as disclosed in Applicants' admitted prior art (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, to implement Bitar system with an IA-64 processor and still able to perform the intended functions equally well without causing the system to crash.

23. Regarding **claim 23,** Bitar did not clearly disclose the content of the inconsequential register is corrupted during the context switch. Nevertheless, this limitation has been disclosed in AAPA as a well-known feature in which certain registers might be corrupted by context switching process (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate this knowledge with Bitar to be aware of the issue, particularly when perform context switch in an IA-64 processor so that current state of the process can be properly reserved and restored when its execution is resumed again.

24. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bitar et al. (US Pat. 5,872,963), as applied to claim 1, in view of Applicants' admitted prior art, and further

in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563, hereinafter Yamaura).

25. Regarding **claims 7 and 8,** as modified Bitar did not clearly disclose the temporary storage includes caller-save register or branch register. Nevertheless, Yamaura discloses a system that use link register (caller-save register) for holding an address of a source from which a subroutine call is made and LI and LN registers (branch register, caller-save register) for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement as modified Bitar's system with Yamaura's teaching with the use of link register and/or branch register as a storage to hold the addresses of the current context information so that data can be accessed more quickly.

26. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bitar et al. (US Pat. 5,872,963), as applied to claim 1 above, and in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563).

27. Regarding **claim 10,** Bitar did not clearly disclose the context is restored by using a branch register to perform an indirect branch. Nevertheless, Yamaura disclose a system that use a plurality of registers for storing data to undergo operation processing which can be freely written/read to/from the registers (page 5, paragraph 0082). Furthermore, Yamaura discloses that LI and LN registers (branch register, caller-save register) are used for holding branch

destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement Bitar's system with Yamaura's teaching with the use of branch register as a storage to hold the destination addresses at a time of IRQ when restoring the context so that processing can be resumed from last interrupt efficiently and quickly.

28. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847) in view of Ooi (US 5,043,878).

29. Regarding **claim 11,** Bugion discloses a method of switching context between a host OS and a virtual machine on a processor (col. 4, lines 52 – 61), the processor having privileged registers (col. 14, lines 1 – 10), the processor having access to other memory (col. 5, lines 6 – 9), the method comprising:

giving the virtual machine access to the privileged registers (col. 14, lines 1 – 10);

using the memory as temporary storage to save the context in other the other memory at a predetermined interruption point (col. 4, lines 46 – 48, col. 11, lines 13 - 15: instructions to be carried out upon occurrence of exception or interrupt. Col. 17, lines 6 – 21. Col. 4, lines 52 – 61: switching from and to between the HOS context and the VMM context is then carried out in the driver and in the virtual machine monitor, respectively. Col. 11, lines 30 – 52: any available memory space may be used to save context and actual storage and retrieval may be accomplished using any known technique, col. 10, lines 31 – 48); and

preventing the processor from changing the context while the context is being saved (col. 11, lines 30 – 52: total switch preferably first saves the state before setting it according to the target context in order to facilitate the inverse operation. Col 17, lines 18 – 21: ensure that no interrupts occur during the switch);

the virtual machine application controlling the context switch (col. 11, lines 30 – 52: VMM handles directly all exceptions and interrupts that occur while executing in the VMM context. Col. 12, lines 20 – 24: the VMM completely takes over the machine and only voluntarily relinquishes control to the HOS).

Bugion did not clearly disclose the context is being saved using the privileged register. Instead, Bugion discloses that any available memory space may be used to save the information and actual storage may be accomplished using any known technique (col. 11, lines 39 – 41). Nevertheless, Ooi discloses the context is being saved with the use of the privileged register (col. 9 lines 22 – 30, col. 7 lines 39 – 47). Therefore, it would have been obvious for one of an ordinary skill in the art, to incorporate Ooi's teaching together with Bugion to utilize the memory and/or the privilege registers as stated to save the context when a context switch occurs and still able to perform the intended functions equally well without causing the system to crash.

30. Claims 12 – 16, 20 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847) in view of Bitar et al. (US Pat. 5,872,963).

31. Regarding **claim 12,** Bugion discloses an apparatus comprising:

a processor including a plurality of registers (col. 14, lines 1 – 10); and

a virtual machine application for commanding the processor to switch context by saving the context under software control (col. 4 lines 46 – 48, col. 11 lines 13 – 15, 30 – 52, col. 17 lines 20 – 21, col. 12 lines 20 - 24) and preventing the processor from changing the context while the context is being saved (col. 11 lines 30 – 52, col. 17 lines 18 – 21).

Bugion did not disclose the use of the inconsequential register as a temporary storage to save the context. Nevertheless, Bitar discloses the use of inconsequential register as storage to save the context during the context switching (col. 13 lines 57 – 65, col. 17 lines 39 – 41, 63 – 65, col. 18 lines 1 – 16). Therefore, it would have been obvious for one of an ordinary skill in the art, to incorporate Bitar's teaching together with Bugion to utilize the memory and/or the registers save area as stated to save the context when a context switch occurs and still able to perform the intended functions equally well without causing the system to crash.

32. Regarding **claim 13,** as modified Bugion discloses the inconsequential register is used as a temporary storage in lieu of a privileged register (Bitar: col. 13 lines 59 - 60).

33. Regarding **claim 14**, as modified Bugion discloses the context is saved at a predetermined interruption point (Bitar: col. 13 lines 53 – 60, col. 17 lines 34 – 58 and 62 – 67).

34. Regarding **claim 15,** as modified Bugion discloses the context is switched between a host operating system and a virtual machine application (Bugion: col. 4, lines 52 – 61: switching from HOS context to VMM context. Col 11, lines 30 – 52), the virtual machine application controlling the context switch (col. 11, lines 30 – 52: VMM handles directly all exceptions and

interrupts that occur while executing in the VMM context. Col. 12, lines 20 – 24: the VMM completely takes over the machine and only voluntarily relinquishes control to the HOS).

35. Regarding **claim 16,** as modified Bugion discloses any available memory space is used to pass information to the virtual machine application (Bugion: col. 11, lines 30 – 52: total switch saves HOS context to any available memory space and changes the address space to be mapped into the VMM context. Col. 16, lines 45 - 61). Bitar discloses the use of inconsequential register to save the context during context switching (col. 13 lines 59 – 60). Therefore, it would have been obvious for one of an ordinary skill in the art, to incorporate Bugion's teaching together with Bitar to utilize the available memory to save the context when a context switch occurs and still able to perform the intended functions equally well without causing the system to crash (Bugion: col. 11 lines 30 – 52).

36. **Claims 20 and 22** are rejected on the same ground as stated in claim 12 above.

37. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847) in view of Bitar et al. (US Pat. 5,872,963), as applied to claim 12 above, and further in view of Applicants' admitted prior art.

38. Regarding **claim 17,** as modified Bugion did not clearly disclose the context switched is using an IA-64 processor. However, an IA-64 processor is considered a well-known architecture as disclosed in Applicants' admitted prior art (specification page 1, paragraph 4). It would have been obvious for one of an ordinary skill in the art, to implement as modified Bugion's system

with an IA-64 processor and still able to perform the intended functions equally well without causing the system to crash.

39. Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847) in view of Bitar et al. (US Pat. 5,872,963), as applied to claim 12 above, in view of Applicants' admitted prior art and further in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563).

40. Regarding **claims 18 and 19,** as modified Bugion did not clearly disclose the temporary storage includes caller-save register or branch register. Nevertheless, Yamaura discloses a system that use link register (caller-save register) for holding an address of a source from which a subroutine call is made and LI and LN registers (branch register, caller-save register) for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement as modified Bugion's system with Yamaura's teaching with the use of link register and/or branch register as a storage to hold the addresses of the current context information so that data can be accessed more quickly.

41. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bugion et al. (US 6,496,847) in view of Bitar et al. (US Pat. 5,872,963), as applied to claim 12 above, and further in view of Yamaura et al. (US. Pat. Application Publication 2001/0008563).

42. Regarding **claim 21,** as modified Bugion did not clearly disclose the context is restored by using a branch register to perform an indirect branch. Nevertheless, Yamaura disclose a system that use a plurality of registers for storing data to undergo operation processing which can be freely written/read to/from the registers (page 5, paragraph 0082). Furthermore, Yamaura discloses that LI and LN registers (branch register, caller-save register) are used for holding branch destination addresses at a time of IRQ (page 6, paragraph 0110 and page 12, paragraph 209, page 5, paragraph 0082). It would have been obvious for one of an ordinary skill in the art, at the time the invention was made, to particularly implement as modified Bugion's system with Yamaura's teaching with the use of branch register as a storage to hold the destination addresses at a time of IRQ when restoring the context so that processing can be resumed from last interrupt efficiently and quickly.

Response to Arguments

43. Applicant's arguments with respect to claims 1, 11, 12 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Thursday 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Lilian Vo
Examiner
Art Unit 2195

ln
December 7, 2006

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